A W-BAND DOUBLER/AMPLIFIER CHAIN USING A MMIC VARACTOR DOUBLER AND A MMIC POWER MESFET AMPLIFIER

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Abstract

A monolithic microwave integrated circuit (MMIC) W-band varactor doubler has been developed that delivers 30 mW of output power at 93 GHz with 12 percent conversion efficiency. U-band MMIC MESFET power amplifier chips were also developed that exhibit 0.23 W of output power with 13 dB of gain from 45.5 to 46.5 GHz. A doubler/amplifier chain has been integrated to deliver 30 mW of output power at 93 GHz with an overall gain of 7 dB.

INTRODUCTION

Missile seekers and phased array radars that operate at 94 GHz require W-band monolithic power transmitters. For such applications, psuedomorphic InGaAs high electron mobility transistors (PM-HEMTs) with multi-quantum well structures and InP-HEMTs show excellent potential for power amplification at W-band (1–3). However, these devices require gate lengths of less than 0.2 μm, which result in a relatively low yield. Moreover, their reliability has yet to be established for power applications. Monolithic power amplifiers using MESFETs with a 0.35-μm gate length, on the other hand, have exhibited output power levels as high as 0.5 W at U-band (4). Therefore, the option of doubling 47 GHz of power to 94 GHz using an efficient monolithic doubler is quite attractive, especially because the yield and reliability are high for such chips. In this paper, we demonstrate the use of state-of-the-art U-band MMIC power MESFET amplifier chips in conjunction with a state-of-the-art W-band MMIC varactor doubler to generate 30 mW of output power at W-band. The developed monolithic amplifier chips use 0.35-μm gate-length molecular beam epitaxy (MBE) MESFET technology and have exhibited 0.23 W of output power with 13 dB of gain and 8 percent power-added efficiency (PAE) from 45.5 to 46.5 GHz. The doubler chip uses a 14-μm diameter vertical varactor diode that has a buried n^+ layer and has exhibited 30 mW of output power at 93 GHz with 12 percent conversion efficiency.

U-BAND AMPLIFIER CHIP DESIGN

Two types of amplifier chips were developed: a driver chip that utilizes a 0.4-mm FET and a power chip that utilizes two 0.4-mm FET devices combined in parallel. The baseline monolithic driver chip design consists of a single-stage, 0.4-mm FET power amplifier with DC blocking capacitors and on-chip bias and stabilization networks. The schematic of the chip design is shown in Figure 1.

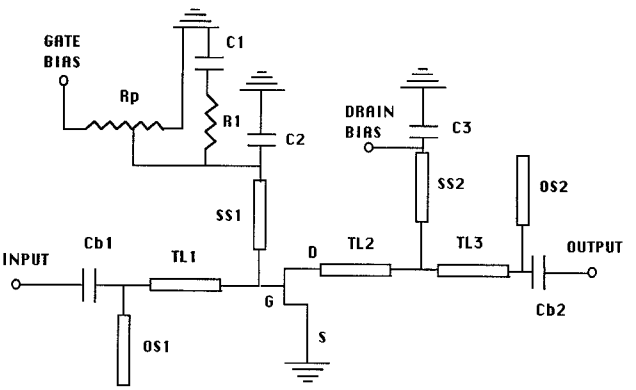

Figure 1. Schematic Diagram of the Driver Chip Circuit

The power chip consisted of two driver chips combined in parallel using integrated Wilkinson type divider/combiner circuits. A small signal-equivalent circuit was obtained for the MESFET device by matching its measured S-parameters to its equivalent circuit S-parameters. The optimum load impedance required by the MESFET device to deliver its maximum output power at 47 GHz was calculated with a load pull program that uses the device equivalent circuit and its DC parameters in the calculation process as described in (5). In the MMIC circuit design, the output matching circuit presented the optimum output impedance to the MESFET in its bandwidth of operation, thus achieving maximum power in that bandwidth. The input matching circuit was designed by conjugate matching the MESFET input impedance with that device, terminated with the optimum load impedance to achieve maximum gain. The source and load match were then optimized for input return loss and gain flatness across the bandwidth of operation by using the Touchstone microwave circuit analysis program. The input matching circuit

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consists of a shorted stub (SS1), a series transmission line (TL1), and an open stub (OS1). The output matching circuit consists of a series transmission line (TL2), a shorted stub (SS2), another series transmission line (TL3), and an open stub (OS2). DC blocking capacitors (Cb1 and Cb2) were included at the input and output of the chip, respectively, to enable direct cascading of the amplifier stages. A stabilizing RC circuit (R1, C1, and C2) was integrated with the gate bias network to ensure unconditional stability of the chip operation down to the MHz frequency range. A potential divider circuit (Rp) was also included at the input to the gate of the FET to scale the available power supply voltage of -5 V of the system to a nominal value of -0.8 V. At the drain side, the +5 V power supply voltage of the system was applied without scaling to the bias circuit of the drain. In the microstrip implementation, narrow transmission lines were avoided to minimize mm-wave circuit losses. A microphotograph of the two chips is shown in Figure 2. The driver chip area is 0.94 x 1.1 mm, while the power chip area is 1.96 x 1.96 mm.

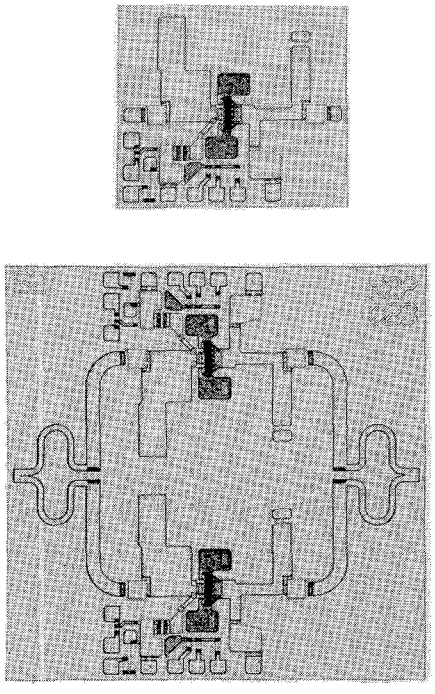

Figure 2. Microphotograph of the U-Band MMIC Driver Amplifier Chip (Chip A) and the Power Amplifier Chip (Chip B)

W-BAND VARACTOR DOUBLER CHIP DESIGN

The doubler circuit, which incorporates a series connected varactor configuration (6), was designed using the multiplier analysis program GISSMIX (7), which performs a nonlinear analysis on the multiplier equivalent circuit to obtain large signal voltage, current, capacitance, and conductance waveforms of the diode. The program requires the diode equivalent circuit, its DC parameters, and the circuit embedding impedances at the pump frequency and four of its harmonics. An equivalent circuit model of the diode was obtained by theoretical analysis of its geometry and material characteristics. As the input and output circuits of the diode are not isolated from each other, it is not possible to optimize each of them independently. Instead, the following iterative design procedure was adopted: first, assume that the output circuit shorts out the fundamental frequency and all of the higher-order harmonics except the second harmonic, while the input circuit shorts out all of the higher-order harmonics except the fundamental frequency. At an arbitrary input power level and using the GISSMIX program, vary the embedding impedance at the second harmonic to find the maximum conversion efficiency. Next, set the embedding impedance at the fundamental to match the input impedance of the diode to 50 ohms. Then, vary the input power level and repeat the above two steps until the maximum conversion efficiency is obtained. Finally, vary the higher-order harmonic embedding impedances to further maximize the efficiency, thus completing the optimization process for that particular diode.

The diode anode area can be scaled to get the required output power with the same efficiency provided that all of the embedding impedances are also scaled accordingly. After the optimization process was completed, the required diameter of the diode anode was determined to be 14 μm, which provided the maximum conversion efficiency at an input power level of 200 mW at 47 GHz. The equivalent circuit of the doubler is shown in Figure 3.

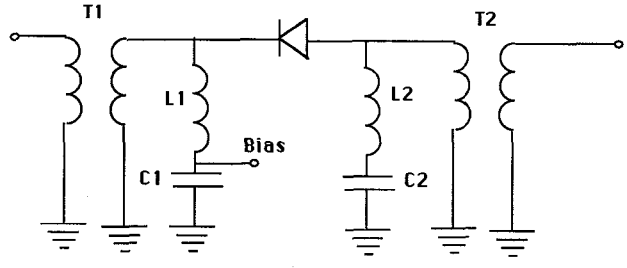

Figure 3. Equivalent Circuit of the W-Band MMIC Doubler

The output matching circuit, represented by transformer T2, was designed to provide optimum impedance to the diode at 94 GHz to deliver maximum power. The fundamental frequency (47 GHz) is shorted at the diode output terminal using an open stub, represented by resonant circuit C2 and L2, which is open at the second harmonic frequency (94 GHz). The input matching circuit, represented by transformer T1, matches the input diode impedance to the source impedance of 50 ohms at 47 GHz. A shorted stub, represented by resonant circuit C1 and L1, shorts the second harmonic frequency at the diode input. The reverse bias is applied to the diode through the input shorted stub. A microphoto-

graph of the chip is shown in Figure 4. The chip area is 0.63 x 1.05 mm.

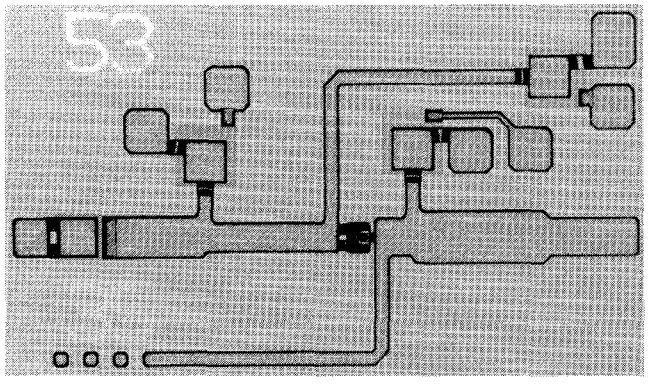

Figure 4. Microphotograph of the W-Band MMIC Doubler Chip

MMIC FABRICATION

The amplifier circuits were fabricated on MBE-grown wafers using a mesa isolation process. The gates were directly written using e-beam lithography. An Au/Ge/Ni/Ag/Au alloy was used for the ohmic contact, and Ti/Pt/Au metallization for the gates. The doubler circuit was similarly fabricated, but on a vapor phase epitaxy (VPE) substrate that had a buried n^+ layer to minimize the diode series resistance. Si_3N_4 was used for both the capacitors dielectric and chip passivation. Following completion of the circuits through the front side, via holes were etched in the thinned wafer. Gold was then plated onto the backside and via holes to a thickness of 10 μm prior to dicing the chips.

MEASURED RESULTS

The doubler was RF tested by mounting the chip in a specially developed test fixture that consisted of input U-band and output W-band microstrip-to-waveguide transitions. The measured output power ranged from 8 to 25 mW across the frequency band of 92 to 95 GHz with an input power of 200 mW, as shown in Figure 5. On the same figure, the predicted output power is plotted vs the output frequency, and it can be seen that reasonable agreement exists between the predicted and measured results. The discrepancy seen was attributed to a higher series resistance of the diode than that considered in the design.

The P_{in} vs P_{out} curve at 93 GHz is shown in Figure 6, and on the same figure, the P_{in} vs conversion efficiency curve is plotted at the same frequency. It can be seen that an output power of 30 mW was obtained at 93 GHz with a conversion efficiency of 12 percent. The reverse bias applied to the varactor diode was 5 V, and the diode current did not exceed 1.5 mA at any data point. The MMIC amplifier chips were tested by mounting them on a test fixture consisting of a pair of U-band waveguide-to-microstrip transitions. Performance

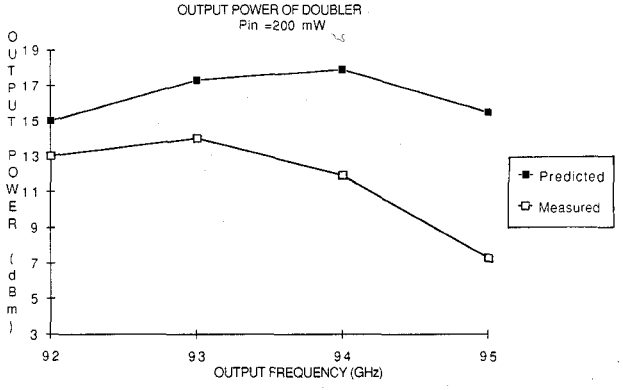

Figure 5. Output Power vs Frequency of W-Band Doubler

of an eight-stage amplifier is shown in Figure 7. The two-output dual-stages were combined externally with Wilkinson combiners/dividers. The amplifier exhibited up to 230 mW of output power with 13 dB of gain from 45.5 to 46.5 GHz. The corresponding PAE was 8 percent.

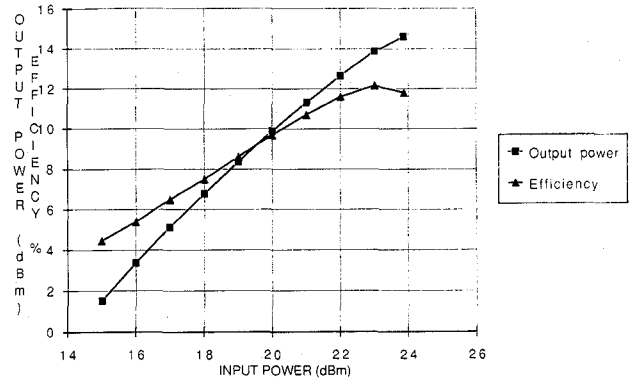

Figure 6. Measured Output Power and Efficiency vs Input Power of Doubler at 93 GHz

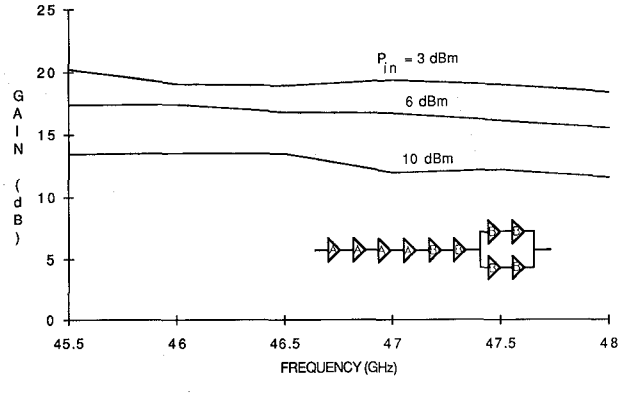

Figure 7. Measured Performance of an Eight-Stage Combined U-Band MMIC Power Amplifier

To construct the doubler/amplifier chain, the above amplifier was used to directly drive the varactor doubler. The assembly of the unit is shown in Figure 8; it consists of an

input U-band microstrip-to-waveguide transition and an output W-band transition. The chips are mounted on carriers that are inserted between the two transitions. The resulting performance of the chain, shown in Figure 9, includes the loss of the connecting 50-Ω lines. As seen from that figure, an output power of 30 mW was obtained at 93 GHz, with an overall gain of 7 dB for the doubler/amplifier chain. According to the same figure, the input power can be backed off to 0 dBm to obtain an output power of 25 mW with an overall gain of 14 dB at the same frequency.

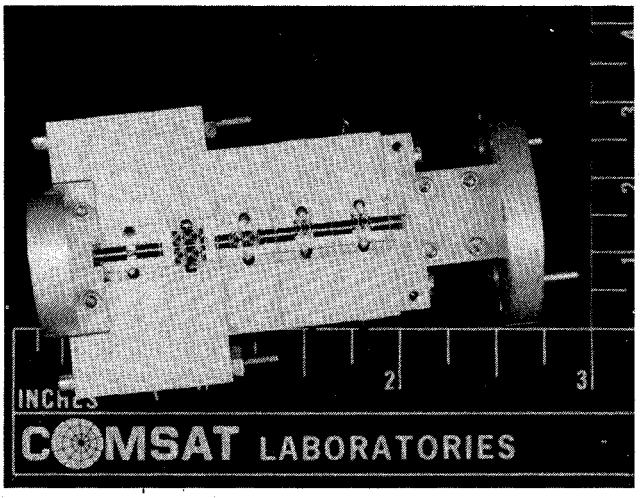

Figure 8. Assembly of the W-Band Doubler/Amplifier Chain

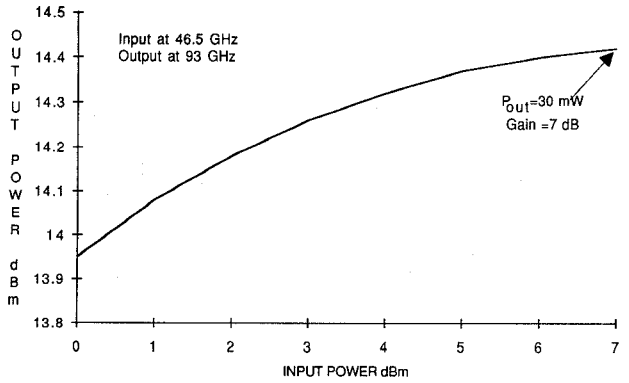

Figure 9. Measured Performance of Doubler/Amplifier Chain

CONCLUSION

The results of a W-band monolithic varactor frequency doubler and U-band MMIC power amplifier chips were reported and establish the feasibility of generating W-band power using a monolithic doubler circuit approach. The bandwidth of the doubler exceeded 4 GHz. At 93 GHz, an output power of 30 mW was obtained with a conversion efficiency of 12 percent. Further improvement in the conversion efficiency is expected by a reduction in the series resistance of the diode. The U-band amplifier exhibited up to 0.23 W of output power with 13 dB of gain and 8 percent PAE from 45.5 to 46.5 GHz. A two-way combined amplifier driving the monolithic doubler exhibited 30 mW of output power at 93 GHz with an overall gain of 7 dB for the doubler/amplifier chain. These chips are applicable for 94-GHz systems that require power transmitters, such as missile seekers and phased arrays.

ACKNOWLEDGMENTS

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